KEITHLEY

Application Note Series

Number 2896

C-V Characterization of MOS Capacitors Using the Model 4200-SCS Semiconductor Characterization System

Introduction

Maintaining the quality and reliability of gate oxides of MOS structures is a critical task in a semiconductor fab. Capacitance-voltage (C-V) measurements are commonly used in studying gate-oxide quality in detail. These measurements are made on a two-terminal device called a MOS capacitor (MOS cap), which is basically a MOSFET without a source and drain. C-V test results offer a wealth of device and process information, including bulk and interface charges. Many MOSdevice parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can also be extracted from the C-V data.

Using a tool such as the Keithley Model 4200-SCS equipped with the 4200-CVU Integrated C-V Option for making C-V measurements on MOS capacitors can simplify testing and analysis. The Model 4200-SCS is an integrated measurement system that can include instruments for both I-V and C-V measurements, as well as software, graphics, and mathematical analysis capabilities. The software incorporates C-V tests, which include a variety of complex formulas for extracting common C-V parameters.

This application note discusses how to use a Keithley Model 4200-SCS Semiconductor Characterization System equipped with the Model 4200-CVU Integrated C-V Option to make C-V measurements on MOS capacitors. It also addresses the basic principles of MOS caps, performing C-V measurements on MOS capacitors, extracting common C-V parameters, and measurement techniques. The Keithley Test Environment Interactive (KTEI) software that controls the Model 4200-SCS incorporates a list of a dozen test projects specific to C-V testing. Each project is paired with the formulae necessary to extract common C-V parameters, such as oxide capacitance, oxide thickness, doping density, depletion depth, Debye length, flatband capacitance, flatband voltage, bulk potential, threshold voltage, metal-semiconductor work function difference, and effective oxide charge. This completeness is in sharp contrast to other commercially available C-V solutions, which typically require the user to research and enter the correct formula for each parameter manually.

Overview Of C-V Measurement Technique

By definition, capacitance is the change in charge (Q) in a device that occurs when it also has a change in voltage (V):

$$C \equiv \frac{\Delta Q}{\Delta V}$$

One general practical way to implement this is to apply a small AC voltage signal (millivolt range) to the device under test, and then measure the resulting current. Integrate the current over time to derive Q and then calculate C from Q and V.

C-V measurements in a semiconductor device are made using two simultaneous voltage sources: an applied AC voltage signal (dV_{ac}) and a DC voltage (V_{dc}) that is swept in time, as illustrated in ***Figure 1***.

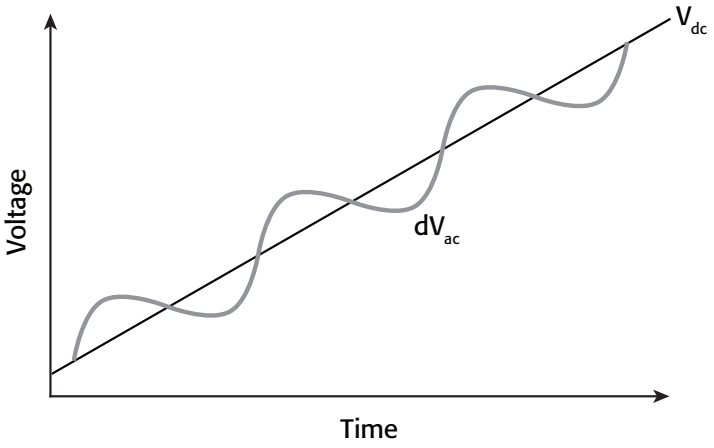


Figure 1. AC and DC voltage of C-V Sweep Measurement

The magnitude and frequency of the AC voltage are fixed; the magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small-signal bias so the capacitance measurement can be performed at a given depth in the device.

Basic Principles of MOS Capacitors

Figure 2 illustrates the construction of a MOS capacitor. Essentially, the MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

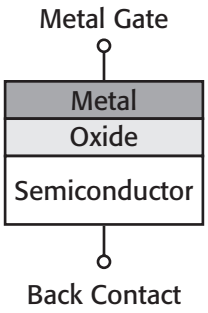


Figure 2. MOS capacitor

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. ***Figure 3*** illustrates a high frequency C-V curve for a p-type semiconductor substrate. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

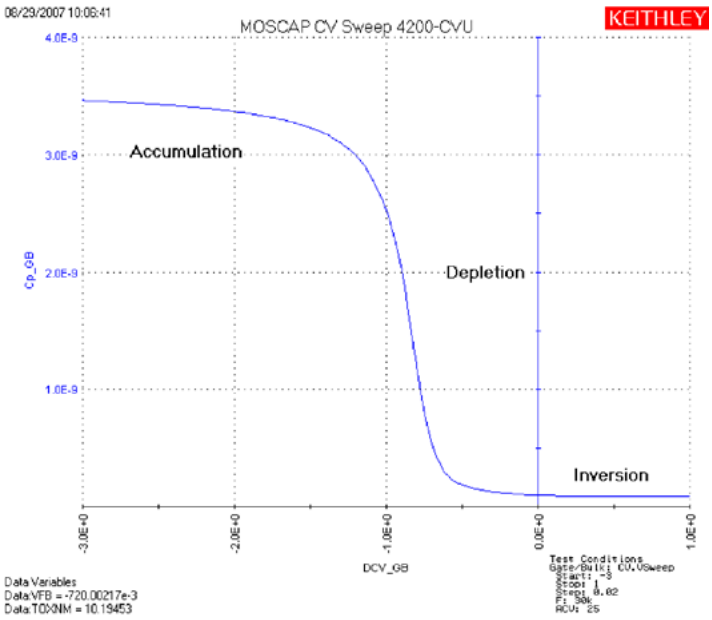


Figure 3. C-V curve of a p-type MOS capacitor measured with the 4200-CVU

The three modes of operation, accumulation, depletion and inversion, will now be discussed for the case of a p-type semiconductor, then briefly discussed for an n-type semiconductor at the end of this section.

Accumulation Region

With no voltage applied, a p-type semiconductor has holes, or majority carriers, in the valence band. When a negative voltage is applied between the metal gate and the semiconductor, more holes will appear in the valence band at the oxide-semiconductor interface. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the semiconductor and the oxide. This state of the p-type semiconductor is called accumulation.

For a p-type MOS capacitor, the oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. However, for a very thin oxide, the slope of the C-V curve doesn't flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance.

Depletion Region

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are replaced from the semiconductor-oxide interface. This state of the semiconductor is called depletion because the surface of the semiconductor is depleted of majority carriers. This area of the semiconductor acts as a dielectric because it can no longer contain or conduct charge. In effect, it becomes an insulator.

The total measured capacitance now becomes the oxide capacitance and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. This decrease in capacitance is illustrated in ***Figure 3*** in the depletion region. As a gate voltage increases, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing the capacitance.

Inversion Region

As the gate voltage of a p-type MOS-C increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. The positive gate voltage generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

Once the depletion region reaches a maximum depth, the capacitance that is measured by the high frequency capacitance meter is the oxide capacitance in series with the maximum depletion capacitance. This capacitance is often referred to as minimum capacitance. The C-V curve slope is almost flat.

NOTE: *The measured inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. Therefore, C-V curves measured at different frequencies may have different appearances. Generally, such differences are more significant at lower frequencies and less significant at higher frequencies.*

n-type Substrate

The C-V curve for an n-type MOS capacitor is analogous to a p-type curve, except that (1) the majority carriers are electrons instead of holes; (2) the n-type C-V curve is essentially a mirror

image of the p-type curve; (3) accumulation occurs by applying a positive voltage to the gate; and (4) the inversion region occurs at negative voltage.

Performing C-V Measurements with the 4200-CVU

To simplify testing, a project has been created for the 4200-SCS that makes C-V measurements on a MOS capacitor and extracts common measurement parameters such as oxide thickness, flat-band voltage, threshold voltage, etc. The project (*CVU_MOScap*) is included with all 4200-SCS systems running KTEI Version 7.0 or later. ***Figure 4*** is a screen shot of the project, which has three tests, called ITMs (Interactive Test Modules), which generate a C-V sweep (*CVSweep_MOScap*), a $1/C^2$ vs. Gate Voltage curve (*C-2vsV_MOScap*), and a doping profile (*DopingProfile_MosC*). ***Figure 4*** also illustrates a C-V sweep generated with the *(CVSweep_MOScap)* test module. All of the extracted C-V parameters in these test modules are defined in the next section of this application note.

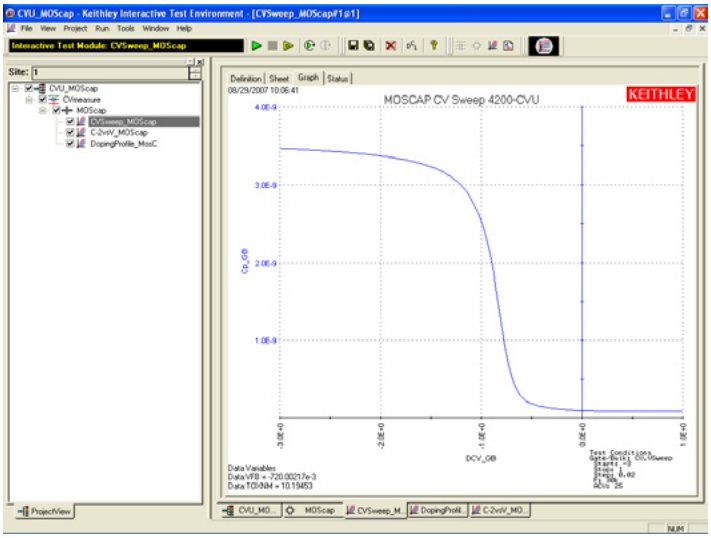


Figure 4. C-V Sweep created with MOScap project for the 4200

CVSweep_MOScap Test Module

This test performs a capacitance measurement at each step of a user-configured linear voltage sweep. A C-V graph is generated from the acquired data, and several device parameters are calculated using the Formulator, which is a tool in the 4200-SCS's software that provides a variety of computational functions, common mathematical operators, and common constants. ***Figure 5*** shows the window of the Formulator. These derived parameters are listed in the Sheet Tab of the Test Module.

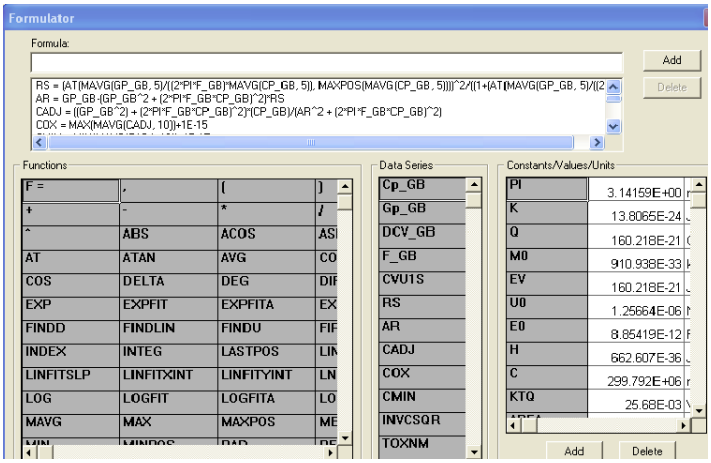


Figure 5. Formulator window with parameters derived

C-2vsV_MOScap Test Module

This test performs a C-V sweep and displays the capacitance ($1/C^2$) as a function of the gate voltage (V_G). This sweep can yield important information about doping profile because the substrate doping concentration (N_{SUB}) is inversely related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. A positive slope indicates acceptors and a negative slope indicates donors. The substrate doping concentration is extracted from the slope of the $1/C^2$ curve and is displayed on the graph. ***Figure 6*** shows the results of executing this test module.

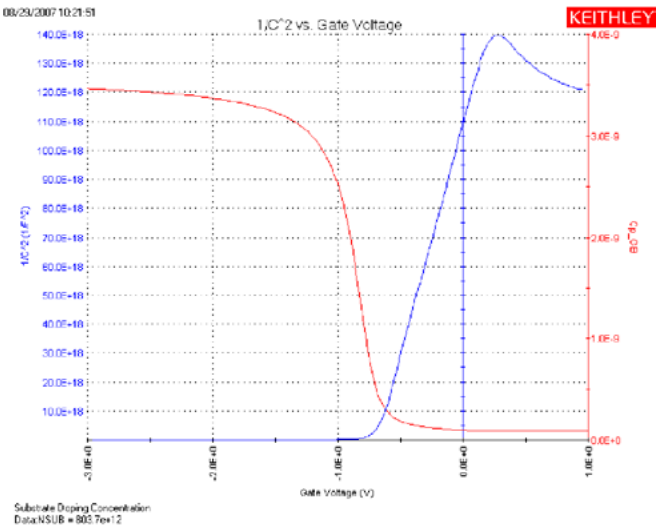


Figure 6. $1/C^2$ vs. gate voltage plot generated with 4200-CVU

DopingProfile Test Module

This test performs a doping profile, which is a plot of the doping concentration vs. depletion depth. The difference in capacitance at each step of the gate voltage is proportional to the doping concentration. The depletion depth is computed from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage. The results are plotted on the graph as shown in ***Figure 7***.

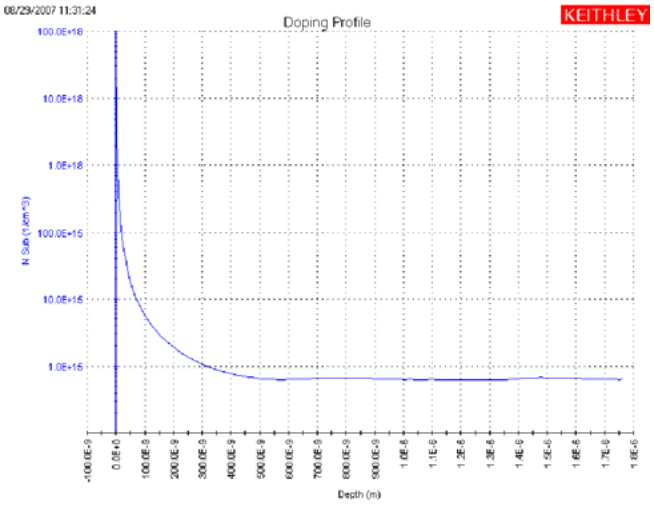


Figure 7. Doping profile extracted from C-V data taken with 4200-CVU

Connections to the 4200-CVU

To make a C-V measurement, a MOS cap is connected to the 4200-CVU as shown in ***Figure 8***. In the ITM, both the 4200-CVU ammeter and the DC voltage appear at the HCUR/HPOT terminals. See the next section, "Measurement Optimization," for further information on connecting the CVU to the device on a wafer.

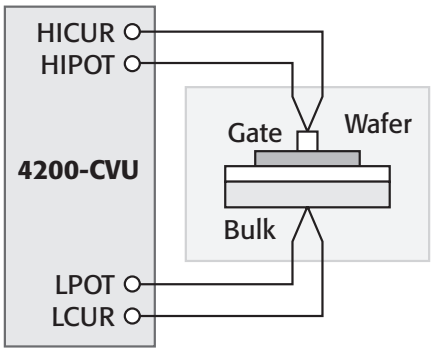


Figure 8. Basic configuration to test MOS capacitor with 4200-CVU

Measurement Optimization

Successful measurements require compensating for stray capacitance, measuring at equilibrium conditions, and compensating for series resistance.

Offset Correction for Stray Capacitance

C-V measurements on a MOS capacitor are typically performed on a wafer using a prober. The 4200-CVU is designed to be connected to the prober via interconnect cables and adaptors and may possibly be routed through a switch matrix. This cabling and switch matrix will add stray capacitance to the measurements.

To correct for stray capacitance, the KTEI software environment has a built-in tool for offset correction, which is a two-part process: the corrections for OPEN and/or SHORT are performed first, and then they can be enabled within an ITM.

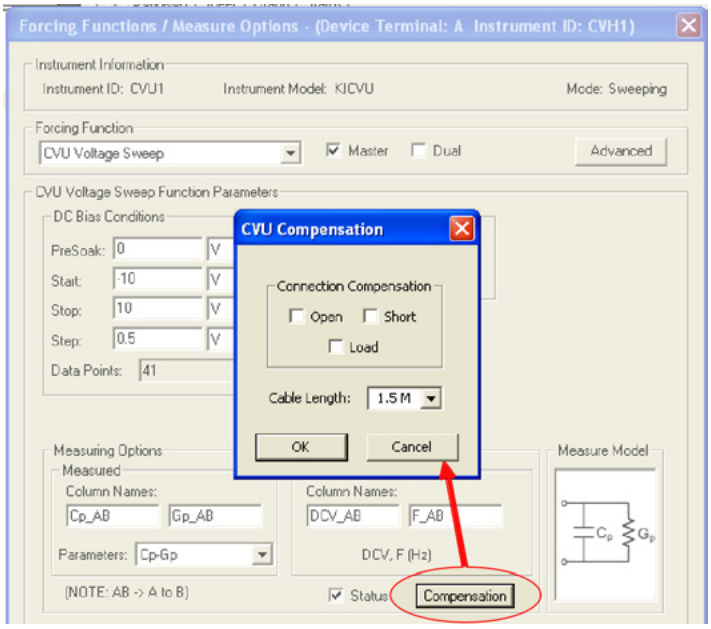


Figure 9. CVU compensation window

To perform the corrections, Open the Tools Menu and select CVU Connection Compensation. For an Open correction, click on Measure Open. Probes must be up during the correction. Open is typically used for high impedance measurements (<10pF or >1MΩ).

For a Short correction, click on Measure Short. Short the probe to the chuck. A short correction is generally performed for low impedance measurements (>10nF or <10Ω).

After the corrections are performed, they must be enabled in the project. To enable corrections, click the Compensation button at the bottom of the Forcing Functions/Measure Options Window. In the CVU Compensation dialog box (***Figure 9***), click only the corrections to be applied.

Measuring at Equilibrium Conditions

A MOS capacitor takes time to become fully charged after a voltage step is applied. C-V measurement data should only be recorded after the device is fully charged. This condition is called the equilibrium condition. Therefore, to allow the MOS capacitor to reach equilibrium: (1) allow a sufficient Hold Time in the Timing Menu to enable the MOS capacitor to charge up while applying a "PreSoak" voltage, and (2) allow a sufficient Sweep Delay Time in the Timing Menu before recording the capacitance after each voltage step of a voltage sweep. The appropriate Hold and Delay Times are determined experimentally by generating capacitance vs. time plots and observing the time for the capacitance to settle.

Although C-V curves swept from different directions may look different, allowing adequate Hold and Delay Times minimizes such differences. One way to determine sufficient Hold and Delay Times is to generate a series of C-V curves in both directions. Change the Hold and Delay Times for each pair of inver-

sion → accumulation and accumulation → inversion curves until the curves look essentially the same for both sweep directions.

Hold and Delay Times When Sweeping from Inversion → Accumulation. When the C-V sweep starts in the inversion region and the starting voltage is initially applied, a MOS capacitor is driven into deep depletion. Thereafter, if the starting voltage is maintained, the initial high frequency C-V curve climbs toward and ultimately stabilizes to the minimum capacitance at equilibrium. However, if the initial Hold Time is too short, the MOS capacitor cannot adequately recover from deep depletion, and the measured capacitance will be smaller than the minimum capacitance at equilibrium. Set the "PreSoak" voltage to the first voltage in the voltage sweep and allow a sufficient Hold Time for the MOS capacitor to reach equilibrium.

However, once the MOS capacitor has reached equilibrium after applying the "PreSoak" voltage, an inversion → accumulation C-V sweep may be performed with small delay times. This is possible because minority carriers recombine relatively quickly as the gate voltage is reduced. Nonetheless, if the Delay Time is too short, non-equilibrium occurs, and the capacitance in the inversion region is slightly higher than the equilibrium value. This is illustrated by the upper dotted line in ***Figure 10***.

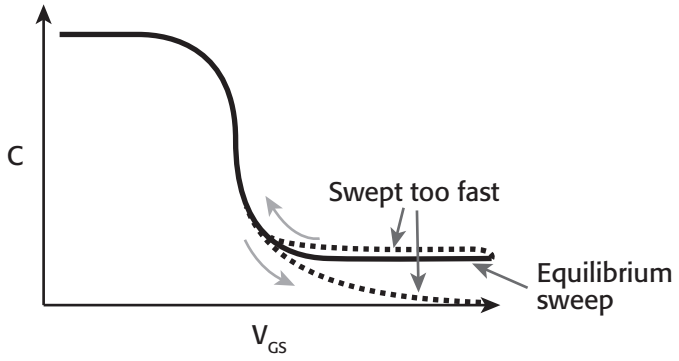


Figure 10. Effects of performing a C-V sweep too quickly

Hold and Delay Times When Sweeping from Accumulation → Inversion. When the C-V sweep starts in the accumulation region, the effects of Hold and Delay Times in the accumulation and depletion regions are fairly subtle. However, in the inversion region, if the Delay Time is too small (i.e., the sweep time is too fast), there's not enough time for the MOS capacitor to generate minority carriers to form an inversion layer. On the high frequency C-V curve, the MOS capacitor never achieves equilibrium and eventually becomes deeply depleted. The measured capacitance values fall well below the equilibrium minimum value. The lower dotted line in ***Figure 10*** illustrates this phenomenon.

Using the preferred sequence. Generating a C-V curve by sweeping from inversion to accumulation is faster and more controllable than sweeping from accumulation to inversion. ***Figure 11*** illustrates a preferred measurement sequence.

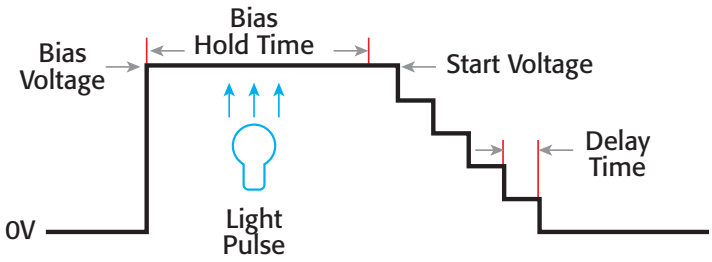


Figure 11. Preferred C-V measurement Sequence

The device is first biased at the "PreSoak" voltage for the Hold Time that is adjusted in the Timing Menu. The bias or "PreSoak" voltage should be the same as the sweep start voltage to avoid a sudden voltage change when the sweep starts. During biasing, if necessary, a short light pulse can be applied to the sample to help generate minority carriers. However, before the sweep starts, all lights should be turned off. All measurements should be performed in total darkness because the semiconductor material may be light sensitive. During the sweep, the Delay Time should be chosen to create the optimal balance between measurement speed and measurement integrity, which requires adequate equilibration time.

Compensating for series resistance

After generating a C-V curve, it may be necessary to compensate for series resistance in measurements. The series resistance (R_{SERIES}) can be attributed to either the substrate (well) or the backside of the wafer. For wafers typically produced in fabs, the substrate bulk resistance is fairly small (<10Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve. Without series compensation, the measured capacitance can be lower than the expected capacitance, and C-V curves can be distorted. Tests for this project compensate for series resistance using the simplified three-element model shown in ***Figure 12***. In this model, C_{OX} is the oxide capacitance and C_A is the capacitance of the accumulation layer. The series resistance is represented by R_{SERIES}.

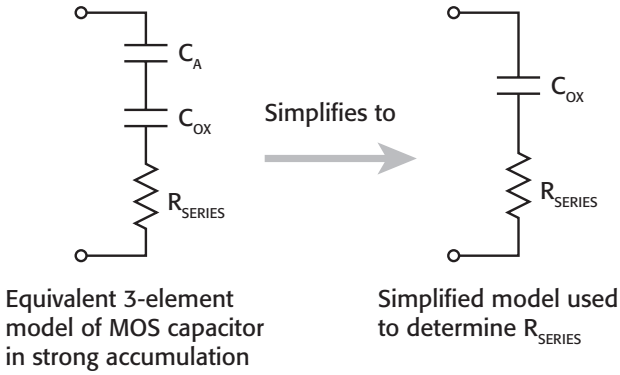


Figure 12. Simplified Model to determine series resistance

The corrected capacitance (C_{ADJ}) and corrected conductance (G_{ADJ}) are calculated from the following formulas [1]:

$$C_{ADJ} = \frac{(G^2 + (2\pi fC)^2)C}{a_R^2 + (2\pi fC)^2}$$

$$G_{ADJ} = \frac{(G^2 + (2\pi fC)^2)a_R}{a_R^2 + (2\pi fC)^2}$$

where:

$a_R = G - (G^2 + (2\pi fC)^2)R_S$

C_{ADJ} = series resistance compensated parallel model capacitance

C = measured parallel model capacitance

G_{ADJ} = series resistance compensated conductance

G = measured conductance

f = test frequency as set in the KITE Definition Tab

R_S = series resistance

The series resistance (R_S) may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) in the accumulation region as follows:

$$R_S = \frac{\left(\frac{G}{2\pi fC}\right)^2}{\left[1+\left(\frac{G}{2\pi fC}\right)^2\right]G}$$

where:

R_S = series resistance

G = measured conductance

C = measured parallel model capacitance (in strong accumulation)

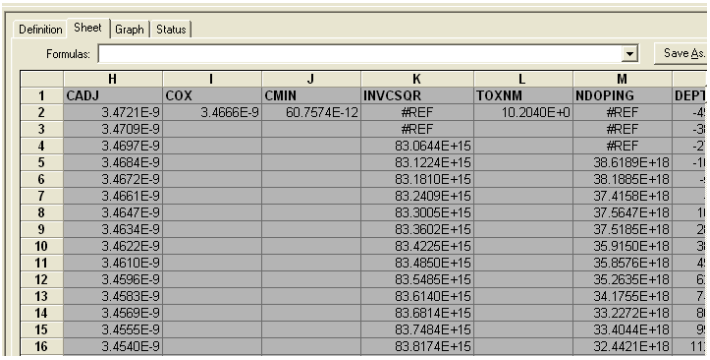
f = test frequency as set in KITE (Definition tab)

NOTE: *The preceding equations for compensating for series resistance require that the Model 4200-CVU be using the parallel model (Cp-Gp).*

For this project, these formulas have been added into the KITE Formulator so the capacitance and conductance can be automatically compensated for the series resistance.

Extracting MOS Device Parameters From C-V Measurements

This section describes the device parameters that are extracted from the C-V data taken in the three test modules in the CVU_MOScap project. The parameters are derived in the Formulator and the calculated values appear in the Sheet tab of each test module as shown in ***Figure 13***.



	H	I	J	K	L	M	
1	CADJ	COX	CMIN	INVCSQR	TOXNM	NDOPING	DEPT
2	3.4721E-9	3.4666E-9	60.7574E-12	#REF	10.2040E+0	#REF	-4
3	3.4709E-9			#REF		#REF	-3
4	3.4697E-9			83.0644E+15		#REF	-2
5	3.4684E-9			83.1224E+15		38.6189E+18	-1
6	3.4672E-9			83.1810E+15		38.1885E+18	
7	3.4661E-9			83.2409E+15		37.4158E+18	
8	3.4647E-9			83.3005E+15		37.5647E+18	1
9	3.4634E-9			83.3602E+15		37.5185E+18	2
10	3.4622E-9			83.4225E+15		35.9150E+18	3
11	3.4610E-9			83.4850E+15		35.8576E+18	4
12	3.4596E-9			83.5485E+15		35.2635E+18	6
13	3.4583E-9			83.6140E+15		34.1755E+18	7
14	3.4569E-9			83.6814E+15		33.2272E+18	8
15	3.4555E-9			83.7484E+15		33.4044E+18	9
16	3.4540E-9			83.8174E+15		32.4421E+18	11

Figure 13. Extracted C-V parameters shown in sheet tab

Oxide thickness

For a relatively thick oxide (>50Å), extracting the oxide thickness is fairly simple. The oxide capacitance (C_{OX}) is the high frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS-C acts like a parallel-plate capacitor, and the oxide thickness (T_{OX}) may be calculated from C_{OX} and the gate area using the following equation:

$$T_{OX(nm)} = \frac{(10^7)A\varepsilon_{ox}}{C_{ox}}$$

where:

T_{OX} = oxide thickness (nm)

A = gate area (cm^2)

ε_{OX} = permittivity of the oxide material (F/cm)

C_{OX} = oxide capacitance (F)

10^7 = units conversion from cm to nm

Flatband capacitance and flatband voltage

Application of a certain gate voltage, the flatband voltage (V_{FB}), results in the disappearance of band bending. At this point, known as the flatband condition, the semiconductor band is said to become flat. Because the band is flat, the surface potential is zero (with the reference potential being taken as the bulk potential deep in the semiconductor). Flatband voltage and its shift are widely used to extract other device parameters, such as oxide charges.

V_{FB} can be identified from the C-V curve. One way is to use the flatband capacitance method. For this method, the ideal value of the flatband capacitance (C_{FB}) is calculated from the oxide capacitance and the Debye length. The concept of Debye length is introduced later in this section. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C-V curve data, by interpolating between the closest gate-to-substrate (V_{GS}) values [2].

The Debye length parameter (λ) must also be calculated to derive the flatband voltage and capacitance. Based on the doping profile, the λ calculation requires one of the following doping concentrations: N at 90% of W_{MAX} (refer to Nicollian and Brews), a user-supplied N_A (bulk doping concentration for a p-type,

acceptor, material), or a user-supplied N_D (bulk doping concentration for an n-type, donor, material).

***NOTE:** The flatband capacitance method is invalid when the interface trap density (D_{IT}) becomes very large (10^{12}–10^{13} or greater). However, the method should give satisfactory results for most users. When dealing with high D_{IT} values, consult the appropriate literature for a more suitable method.*

The flatband capacitance is calculated as follows:

$$C_{FB} = \frac{C_{ox}\ (\varepsilon_S A/\lambda)\ (10^2)}{C_{ox} + (\varepsilon_S A/\lambda)\ (10^2)}$$

where:

C_{FB} = flatband capacitance (F)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

A = gate area (cm^2)

10^2 = units conversion from m to cm

λ = extrinsic Debye length, which is calculated as follows:

$$\lambda = \left(\frac{\varepsilon_S kT}{q^2 N}\right)^{1/2} (10^{-2})$$

where:

λ = extrinsic Debye length

ε_S = permittivity of the substrate material (F/cm)

kT = thermal energy at room temperature (293K) (4.046×10^{-21}J)

q = electron charge (1.60219×10^{-19}C)

$N_X = N$ at 90% W_{MAX} or N90W (refer to Nicollian and Brews; see References) or, when input by the user, $N_X = N_A$ or $N_X = N_D$

10^{-2} = units conversion from cm to m

The extrinsic Debye length is an idea borrowed from plasma physics. In semiconductors, majority carriers can move freely. The motion is similar to a plasma. Any electrical interaction has a limited range. The Debye length is used to represent this interaction range. Essentially, the Debye length indicates how far an electrical event can be sensed within a semiconductor.

Threshold voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot. When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current. When a source and drain are added to a MOS-C to form a MOSFET, a p-type MOS-C becomes an n-type MOSFET, also called an n-channel MOSFET. Conversely, an n-type MOS-C becomes a p-channel MOSFET.

The threshold voltage (V_{TH}) is the point on the C-V curve where the surface potential (ϕ_S) equals twice the bulk potential (ϕ_B). This curve point corresponds to the onset of strong inversion. For an enhancement-mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct. The physical meaning of the threshold voltage is the same for both a MOS-C C-V curve and a MOSFET I-V curve. However, in practice, the numeric V_{TH} value for a MOSFET may be slightly different due to the particular method used to extract the threshold voltage.

The threshold voltage of a MOS capacitor can be calculated as follows:

$$V_{TH} = V_{FB} \pm \left[\frac{A}{C_{OX}}\sqrt{4\varepsilon_S q |N_{BULK}\,\phi_B|} + 2|\phi_B|\right]$$

where:

V_{TH} = threshold voltage (V)

V_{FB} = flatband potential (V)

A = gate area (cm^2)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3}) (Note: The Formulator name for N_{BULK} is N90W.)

ϕ_B = bulk potential (V) (Note: The Formulator name for ϕ_B is PHIB.)

The bulk potential is calculated as follows:

$$\phi_B = -\frac{kT}{q}\ln\left(\frac{N_{BULK}}{N_i}\right)(DopeType)$$

where:

ϕ_B = bulk potential (V) (Note: The Formulator name for ϕ_B is PHIB.)

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = Bulk doping (cm^{-3}) (Note: The Formulator name for N_{BULK} is called N90W.)

N_i = Intrinsic carrier concentration ($1.45 \times 10^{10} cm^{-3}$)

$DopeType$ = +1 for p-type materials and –1 for n-type materials

Metal-semiconductor work function difference

The metal-semiconductor work function difference (W_{MS}) is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge [3][4]. The work function represents the difference in work necessary to remove an electron from the gate and from the substrate. The work function is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_{BG}}{2} - \phi_B\right]$$

where:

W_{MS} = work function

W_M = metal work function (V) *

W_S = substrate material work function, electron affinity (V) *

E_{BG} = substrate material bandgap (V) *

ϕ_B = bulk potential (V) (Note: The Formulator name for ϕ_B is PHIB)

*The values for W_M, W_S, and E_{BG} are listed in the Formulator as constants. The user can change the values depending on the type of materials.

The following example calculates the work function for silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B\right]$$

Therefore,

$$W_{MS} = -0.61 + \varphi_B$$

and

$$W_{MS} = -0.61 - \frac{kT}{q}\ln\left(\frac{N_{BULK}}{N_i}\right)(DopeType)$$

where:

W_{MS} = work function

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3})

DopeType = +1 for p-type materials and –1 for n-type materials

For example, for an MOS capacitor with an aluminum gate and p-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), W_{MS} = –0.95V. Also, for the same gate and n-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), W_{MS} = –0.27V. Because the supply voltages of modern CMOS devices are lower than those of earlier devices and because aluminum reacts with silicon dioxide, heavily doped polysilicon is often used as the gate material. The goal is to achieve a minimal work-function difference between the gate and the semiconductor, while maintaining the conductive properties of the gate.

Effective and total bulk oxide charge

The effective oxide charge (Q_{EFF}) represents the sum of oxide fixed charge (Q_F), mobile ionic charge (Q_M), and oxide trapped charge (Q_{OT}):

$$Q_{EFF} = Q_F + Q_M + Q_{OT}$$

Q_{EFF} is distinguished from interface trapped charge (Q_{IT}), in that Q_{IT} varies with gate bias and Q_{EFF} does not [5] [6]. Simple measurements of oxide charge using C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling [7]. Also, because the charge profile in the oxide is not known, the quantity (Q_{EFF}) should be used as a relative, not an absolute, measure of charge. It assumes that the charge is located in a sheet at the silicon–silicon dioxide interface.

From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}}$$

where:

V_{FB} = flatband potential (V)

W_{MS} = metal-semiconductor work function (V)

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

Note that C_{OX} here is per unit of area. So that:

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

where:

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

W_{MS} = metal–semiconductor work function (V)

V_{FB} = flatband potential (V)

A = gate area (cm^2)

For example, assume a $0.01cm^2$, 50pF, p-type MOS-C with a flatband voltage of –5.95V; its N_{BULK} of $10^{16}cm^{-3}$ corresponds to a W_{MS} of –0.95 V. For this example, Q_{EFF} can be calculated to be $2.5 \times 10^{-8}C/cm^2$, which in turn causes the threshold voltage to shift ~5V in the negative direction. Note that in most cases where the bulk charges are positive, there is a shift toward negative gate voltages. The effective oxide charge concentration (N_{EFF}) is computed from effective oxide charge (Q_{EFF}) and the electron charge as follows:

$$N_{EFF} = \frac{Q_{EFF}}{q}$$

where:

N_{EFF} = effective oxide charge density (cm^{-2})

Q_{EFF} = effective oxide charge (C)

q = electron charge (1.60219×10^{-19}C)

Substrate doping concentration

The substrate doping concentration (N) is related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. The doping concentration is calculated and displayed below the graph in the *C-2vsV_MOScap* test as follows:

$$N_{SUB} = \frac{2}{q\varepsilon_S A^2\left(\frac{\Delta 1/C^2}{\Delta V_G}\right)}$$

where:

N_{SUB} = substrate doping concentration

q = electron charge (1.60219×10^{-19}C)

A = gate area (cm^2)

ε_S = permittivity of the substrate material (F/cm)

V_G = gate voltage (V)

C = measured capacitance (F)

Doping concentration vs. depth (doping profile)

The doping profile of the device is derived from the C-V curve based on the definition of the differential capacitance as the differential change in depletion region charges produced by a differential change in gate voltage [8].

The standard doping concentration (N) vs. depth (w) analysis discussed here does not compensate for the onset of accumulation, and it is accurate only in depletion. This method becomes inaccurate when the depth is less than two Debye lengths. The doping concentration used in the doping profile is calculated as:

$$N = \left| \frac{-2}{q\varepsilon_s A^2 \frac{d(1/C^2)}{dV}} \right|$$

The *CVU_MOScap* project computes the depletion depth (w) from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage (V_G) [9]. The Formulator computes each (w) element of the calculated data array as shown:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}} \right) (10^2)$$

where:

W = depth (m)

A = the gate area (cm^2)

C = the measured capacitance (F)

ε_S = the permittivity of the substrate material (F/cm)

C_{OX} = the oxide capacitance (F)

10^2 = units conversion from cm to m

Once the doping concentration and depletion depth are derived, a doping profile can be plotted. This is done in the Graph tab of the DopingProfile test in the *CVU_MOScap* project.

Summary

When equipped with the 4200-CVU option, the Model 4200-SCS is a very useful tool for making both C-V and I-V measurements on MOS capacitors and deriving many of the common MOS parameters. In addition to the *CVU_MOScap* project, the Model 4200-SCS includes other projects specifically for testing MOS capacitors. The *CVU_lifetime* project is used for determining generation velocity and lifetime testing (Zerbst plot) of MOS capacitors. The *CVU_MobileIon* project determines the mobile charge of a MOS cap using the bias-temperature stress method. In addition to making C-V measurements, the SMUs can make I-V measurements on MOS caps, including leakage current and breakdown testing.

References

1. E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (New York: Wiley, 1982), 224.
2. *Ibid.*, 487–488
3. Nicollian and Brews, 462–477.
4. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition. (New York: Wiley, 1985), 395–402.
5. Nicollian and Brews, 424–429.
6. Sze, 390–395.
7. Nicollian and Brews, 429 (Figure 10.2).
8. Nicollian and Brews, 380–389.
9. Nicollian and Brews, 386.

Additional Suggested Reading

D.K. Schroder, *Semiconductor Material and Device Characterization*, 2nd edition. (New York, Wiley, 1998).

KEITHLEY

KEITHLEY INSTRUMENTS, INC. ■ 28775 AURORA ROAD ■ CLEVELAND, OHIO 44139-1891 ■ 440-248-0400 ■ Fax: 440-248-6168 ■ 1-888-KEITHLEY ■ www.keithley.com

BELGIUM
Sint-Pieters-Leeuw
Ph: 02-363 00 40
Fax: 02-363 00 64
www.keithley.nl

CHINA
Beijing
Ph: 8610-82255010
Fax: 8610-82255018
www.keithley.com.cn

FINLAND
Espoo
Ph: 09-88171661
Fax: 09-88171662
www.keithley.com

FRANCE
Saint-Aubin
Ph: 01-64 53 20 20
Fax: 01-60-11-77-26
www.keithley.fr

GERMANY
Germering
Ph: 089-84 93 07-40
Fax: 089-84 93 07-34
www.keithley.de

INDIA
Bangalore
Ph: 080-26771071-73
Fax: 080-26771076
www.keithley.com

ITALY
Milano
Ph: 02-553842.1
Fax: 02-55384228
www.keithley.it

JAPAN
Tokyo
Ph: 81-3-5733-7555
Fax: 81-3-5733-7556
www.keithley.jp

KOREA
Seoul
Ph: 82-2-574-7778
Fax: 82-2-574-7838
www.keithley.co.kr

MALAYSIA
Penang
Ph: 60-4-656-2592
Fax: 60-4-656-3794
www.keithley.com

NETHERLANDS
Gorinchem
Ph: 0183-63 53 33
Fax: 0183-63 08 21
www.keithley.nl

SINGAPORE
Singapore
Ph: 65-6747-9077
Fax: 65-6747-2991
www.keithley.com.sg

SWEDEN
Solna
Ph: 08-50 90 46 00
Fax: 08-655 26 10
www.keithley.com

SWITZERLAND
Zürich
Ph: 044-821 94 44
Fax: 41-44-820 30 81
www.keithley.ch

TAIWAN
Hsinchu
Ph: 886-3-572-9077
Fax: 886-3-572-9031
www.keithley.com.tw

UNITED KINGDOM
Theale
Ph: 0118-929 75 00
Fax: 0118-929 75 19
www.keithley.co.uk

Printed in the U.S.A. No. 2227 Dec. 07